AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a first die having:

a substrate with an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having:

a micro-electromechanical structure having an inductance;

a plurality of third bonding pads connected to the micro-electromechanical structure , a portion of a third bonding pad being substantially vertically aligned with a portion of a second bonding pad; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

2. (Previously Amended) The integrated circuit of claim 1 and further comprising:

a package, the package having a plurality of fourth bonding pads, a plurality of circuit board connectors, and internal routing that electrically connects the plurality of fourth bonding pads to the plurality of circuit board connectors, the first die being attached to the package; and

a plurality of wires connected to the first bonding pads and the fourth bonding pads.

3. (Previously Amended) The integrated circuit of claim 1 wherein the second die further includes a capacitive micro-electromechanical structure that has a capacitance.

Claims 4-20 (Cancelled).

21. (Previously Presented) The integrated circuit of claim 1 wherein the plurality of connectors includes solder.

22. (Previously Presented) The integrated circuit of claim 1 wherein

the passivation layer has a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

the plurality of first bonding pads are formed on the passivation layer only in the peripheral region; and

the plurality of second bonding pads are formed on the passivation layer only in the center region.

23. (Cancelled).

24. (Previously Presented) The integrated circuit of claim 2 wherein the package has a top surface and a bottom surface, the plurality of fourth bonding pads are located on the top surface, and the plurality of circuit board connectors are located on the bottom surface.

25. (Currently Amended) An integrated circuit comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect, the passivation layer having a top surface, a rectangularly-shaped center region of the top surface, and a peripheral region of the top surface that surrounds the center region, the peripheral region having four interior sides, four exterior sides, and four widths measured from each of the four interior sides to a corresponding exterior side, the four widths being equal;

a plurality of first bonding pads formed on the passivation layer only in the peripheral region, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer only in the center region, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

26. (Currently Amended) ~~The integrated circuit of claim 25 wherein~~ An integrated circuit comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect, the passivation layer having a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

a plurality of first bonding pads formed on the passivation layer only in the peripheral region, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer only in the center region, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads, a portion of a third bonding pad ~~is~~ being substantially vertically aligned with a portion of a second bonding pad; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

27. (Cancelled)

28. (Previously Presented) The integrated circuit of claim 25 wherein the second die includes a micro- electromechanical structure.

29. (Previously Presented) The integrated circuit of claim 28 wherein the micro- electromechanical structure has inductance.

30. (Previously Presented) The integrated circuit of claim 28 wherein the micro-electromechanical structure has capacitance.

31. (Previously Presented) The integrated circuit of claim 28 wherein the first die does not include a micro-electromechanical structure.

32. (Currently Amended) An integrated circuit device comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads;

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads;

a package including:

a substrate having a top surface and a bottom surface, the substrate being attached to the first die; and

a plurality of fourth bonding pads formed on the top surface of the substrate, no other bonding pads being formed on the top surface of the substrate; and

a plurality of bonding wires, the wires directly connecting the first bonding pads to the fourth bonding pads, no bonding wires connecting the second bonding pads to any fourth bonding pads.

33. (Currently Amended) ~~The integrated circuit device of claim 32 wherein~~ An integrated circuit device comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads;

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads;

a package including:

a substrate having a top surface and a bottom surface, the substrate being attached to the first die;

a plurality of fourth bonding pads formed on the top surface of the substrate;

internal routing electrically connected to the fourth bonding pads;

a plurality of circuit board connectors formed on the bottom surface of the substrate, the circuit board connectors being connected to the internal routing, the plurality of circuit board connectors ~~include~~ including solder regions; and

a plurality of bonding wires, the wires connecting the first bonding pads to the fourth bonding pads.

34. (Previously Presented) The integrated circuit device of claim 33 wherein the plurality of circuit board connectors include pins.

35. (Previously Presented) The integrated circuit of claim 33 wherein the plurality of connectors includes solder.

36. (Previously Presented) The integrated circuit of claim 33 wherein the passivation layer has a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

the plurality of first bonding pads are formed on the passivation layer only in the peripheral region; and

the plurality of second bonding pads are formed on the passivation layer only in the center region.

37. (Previously Presented) The integrated circuit of claim 33 wherein a portion of a third bonding pad is substantially vertically aligned with a portion of a second bonding pad.

38. (New) An integrated circuit comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect, the passivation layer having a top surface and a plurality of edges that contact the top surface, the plurality of edges including a first edge, a second edge that opposes the first edge, a third edge, and a fourth edge that opposes the third edge;

a number of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect, a first plurality of first bonding pads lying closest to the first edge, a second plurality of first bonding pads lying closest to the second edge, a third plurality of first bonding pads lying closest to the third edge, a fourth plurality of first bonding pads lying closest to the fourth edge;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect, the first plurality of first bonding pads lying between the second bonding pads and the first edge, the second plurality of first bonding pads lying between the second bonding

pads and the second edge, the third plurality of first bonding pads lying between the second bonding pads and the third edge, the fourth plurality of first bonding pads lying between the second bonding pads and the fourth edge;

a second die having a plurality of third bonding pads; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

39. (New) An integrated circuit comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect, the passivation layer having a top surface and a plurality of edges that contact the top surface, the plurality of edges including a first edge, a second edge that opposes the first edge, a third edge, and a fourth edge that opposes the third edge;

a number of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect; and

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having a top surface, an opposing bottom surface, and a plurality of third bonding pads formed in the bottom surface, the bottom surface lying closer to the first die than the top surface, the top surface being free of any electrical connections; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.